February 13, 1997
GFK-1196D

IMPORTANT PRODUCT INFORMATION

READ THIS INFORMATION FIRST

Product: **PLC CPU Module, Release 6.02**
IC697CPM915-CC

The purpose of this release is to fix the problem listed under *Problems Resolved by This Upgrade*. This hardware change eliminates extremely rare race conditions where CPU programmer port activity with large ladder programs and specific ladder logic can cause a CPU hardware watchdog timeout, or a PLC CPU Hardware Fault. A power cycle is required to recover. In the hardware watchdog timeout case, no faults appear in the fault table.

Release 6.02 is not available for the following IC697 CPUs: IC697CPU731, 732, 771, 772, 780, 788, and 789.

Table 1. Catalog Numbers

New Catalog Number	Replaces
IC697CPM915-CC	IC697CPM915-AA, AB, BB, BC

Identification

Hardware and software identification is summarized in the following tables.

Table 2. Hardware Identification

Catalog Number	Board Identification	Board Revision
IC697CPM915-CC	CPVA1	44A732261-G01 R06 or later (mother board)
	CMVA1	44A735200-G01 R02 or later (memory board)

Table 3. Firmware Identification

Catalog Number	EPROM Location	EPROM/Diskette Label
IC697CPM915-CC	n / a n / a U45	44S750416-G01R07 6.02 (3”) 44S750416-G02R06 6.02 (5”) 388-042A2.00

Compatibility

The new hardware is fully compatible with existing IC697 hardware firmware.

Packaging Note

The user manual is not shipped with every product. User manuals are provided as a complete set in a library with IC641 Programming Software products, are available on CD-ROM, or can be ordered as individual manuals.

Update Information

Update kits are available to update PLC CPUs to version 6.02. Existing units may be updated for a charge by ordering the field update kit. No general field update is planned.

If the failure mode described in *Problems Resolved by This Upgrade* is observed, consult the Technical Support Hotline or Field Service for upgrade information.

Upgrading v6.00 (or v6.01) CPUs

For those customers who purchased a version 6.00 (or 6.01) CPU ***or*** who updated an existing unit by purchasing a version 6.00 (or 6.01) update kit, a free update kit can be obtained by referencing the SPA*"CPU version 6.00 (or version 6.01) to version 6.02 Upgrade SPA*". This is a firmware only upgrade kit, 44A735540-G06 for existing version 6.00 (and 6.01) CPUs.

Update Diskettes Permit Unlimited Installs

The FLASH program update diskettes for upgrading to Release 6.02 CPU firmware now allows unlimited installs (that is, one CPM915 update kit will update any number of CPU915 CPUs to Release 6.02 firmware).

Table 4. Update Kit for Updating CPM915 Firmware

Upgrade Kit	For Upgrading	To
44A735540–G06	IC697CPM915-AA, AB, BB	IC697CPM915-BC

CPM915 Update Available on Bulletin Board Service

The file provided in the update kit listed in Table 4 is now available on the Electronic Bulletin Board Service (BBS). This update kit has been ZIP'ed into a single self-extracting .EXE file and placed in the *PLC:PUBLIC* conference and the *PLC:Series 90-70* directory. Each of the Bulletin Board entries for this update file contains information explaining what the file is and how to create a master update diskette from these files. For those customers who have access to the Electronic Bulletin Board, updates for the CPM915 CPU can be obtained by downloading the appropriate .EXE file. There is no charge for updates obtained in this manner.

Table 5. Bulletin Board Filename for CPM915 Firmware Updates

Upgrade Kit	For Upgrading	To
CPM91602.EXE	IC697CPM915-AA, AB, BB	IC697CPM915-BC

Note

Ensure that you download the correct .EXE file. CPM914/915 firmware will not work on a CPM924/925 and CPM924/925 firmware will not work with a CPM914/915.

Documentation

The following table lists the applicable documentation for the IC697CPM915 CPU.

Table 4. User Documentation

Catalog Number	Data Sheet	User Manual
IC697CPM915-CC	GFK-1119A,or later	see below

Full Documentation Sets

Full documentation sets are also available in either printed / bound form or in electronic form (CD-ROM). Please refer to the following table for ordering information for full documentation sets.

Table 5. Full Documentation Set

Catalog Number	Description
IC697LBR701*	Paperlibrary - full set of printed manuals
IC690CDR002*	CD-ROM - full set of manuals in electronic format

* Current version will be shipped.

Read this document before installing or attempting to use the IC697CPM915 PLC CPU Module. For more information, refer to the applicable *Programmable Controller Installation manual, Programming Software User's Manua*l, and *Programmable Controller Reference Manual*.

Special Operation Notes

IC641 Compatibility

This release of the PLC CPU modules is compatible with the versions of IC641 programming software listed in the table below. However, IC641 version 6.00 or later is required to gain access to all of the CPU's features and functionality. To work around a compatibility problem with serial IC641 programming software, the PLC will return 3.60 as its version to all serial IC641 programming software products (WSI and Standard COM) Release 3.04 and earlier.

CPU Model	IC641 Programming Software
915	Version 6.00 or later

If Release 6.02 PLC CPU firmware is used with IC641 programming software Release 4.01 or 4.02, the PLC Sweep Control and Monitor screen (F3 F8) should **ONLY** be used to change (tune) the constant window or constant sweep time. Any other use may result in the background window time being incorrectly set to 255 milliseconds. For those IC641 programming software releases used with a Release 6.02 CPU, the configuration package must be used to set the desired sweep modes or window times.

Microcycle Mode and First Output Scan

Microcycle mode is a new sweep mode beginning with the release 6.00 CPU. In this mode, the PLC keeps the time interval between I / O scans constant (for a further

description of Microcycle mode see *New Features and Functionality, Microcycle Sweep Mode*) – actually the start of sweep time is maintained as a fixed interval.

In keeping the time interval between I/O scans constant, the CPU must know the amount of the sweep to be allocated to the output scan. Under normal operating situations, the amount of time required to complete the previous sweep's output scan is used to estimate the amount of time required to complete this sweep's output scan.

Obviously, this manner of estimating the amount of time required for the output scan does not work for the first output scan of the IC697 PLC. Since no previous sweep's output scan time is available, the Release 6.xx CPU will estimate the output scan time based upon the configured base cycle time. The first output scan will be estimated as one-third of the configured base cycle time. (that is, if the base cycle time is configured to be 60 milliseconds, then the first output scan will be estimated as requiring 20 milliseconds). When programming for first scan, ensure that the logic to be performed in a given program will complete prior to the next execution time for that same program.

PCM and BTM Compatibility

With the timing improvements and new features first made available in Release 5.00, it is highly recommended that systems using PCMs use IC697PCM711J or later. It is also highly recommended that systems using BTMs use IC697BEM713B or later. Use of boards of an earlier revision may result in lower system performance.

PCM (to CPU) Communications Timeout

The PCM has a default backplane communications timeout value of 5 seconds. After the PCM has sent a request to the IC697 CPU, the PCM applies this timeout while waiting on a response back from the CPU. In most cases, the CPU will respond well within the 5 second timeout, however, in certain instances the CPU can take longer than 5 seconds to respond. *These cases are limited to LOADs and/or STOREs of program and/or configuration - especially if blocks in the program are larger than 8 KBytes. Folders containing EXE blocks (again with *.EXE files >8 KBytes) are most likely to cause problems. Beginning in Release 6.00 Standalone C programs larger than 8 Kbytes also cause this to happen.*

Beginning in Release 5.50 of the IC697 CPUs, the CPU is guaranteed to respond within 8 seconds. To ensure that the PCMs do not observe backplane timeouts, a file must be loaded (using *termf*) to the PCM. The file must be named *CPU.ENV* and is a binary file. The contents of this file are as follows (all values are specified in hexadecimal):

FILE OFFSET	DATA															
0000	4C	5A	01	01	00	00	00	00-00	00	00	00	01	00	00	00	LZ . . . . .
0010	00	00	00	00	00	00	00	00-00	00	43	50	55	4C	49	4E	. . . . . CPULIN
0020	4B	2E	43	4F	44	00	2D	62-00	36	34	00	2D	74	00	32	K . C O D . –b . 6 4 . –t . 2
0030	30	30	00	00	43	50	55	4C-49	4E	4B	2E	44	43	42	00	0 0 . .C P U L I N K . D C B .
0040	00	4E	55	4C	4C	3A	00	4E-55	4C	4C	3A	00	4E	55	4C	. N U L L : . N U L L : . N U L
0050	4C	3A	00	00	00	00	00	00-00	00	00	00	00	00	00	00	L : . . . . .
0060	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .
0070	00	00	00	00	00	00	00	00-00	00	00	00	00	00	00	00	. . . . .

Once the binary file CPU.ENV (above) is created, use *termf* to load CPU.ENV to the PCM. Then execute a soft reset of the PCM. After executing the soft reset, the PCM's backplane communications timeout should be 10 seconds.

Note

A copy of the above CPU.ENV file can be obtained from the Electronic Bulletin Board Service (BBS). CPU.ENV can be found in the *conference:library* of PLC:PCM and is named *CPU.ENV.*

CAUTION

The CPU.ENV file *will not* be used when a hard reset is performed on the PCM. With the CPU.ENV file resident in the PCM, a soft reset must be performed after every hard reset of the PCM. Be aware that it is possible to issue a *soft reset* COMMREQ from the Ladder Diagram application; therefore, the application can be modified to handle the required reset of PCMs after a power cycle of the PLC system

Notice to Upgrade GBC Hardware

With the introduction of new features in CPU Release 5.00, timings with the IC66* Bus Controllers (GBCs / NBCs) have changed; this has uncovered a problem in the GBC / NBC firmware. GBCs / NBCs in expanded racks could be lost if the system is fully configured and only the main rack cycles power.

Also, in previous versions of the GBC / NBC there was a problem with input data coherency. In a system with a large CPU sweep time and a short IC66* bus scan time a problem could be seen if a device is lost. Input data could be defaulted off while the CPU is reading the data from the GBC / NBC.

It is recommended to update existing GBC/NBC hardware to IC697BEM731M or later when updating PLC CPU firmware to Release 6.02. Operation of the IC697BEM731M, in conjunction with Release 6.02 of the IC697CPU will result in a slight impact to the I/O scan time of the PLC.

Third Party VME Modules

IC641 programming software Release 5.00 (and later) allows Third Party VME modules to be configured for six modes: NONE, INTERRUPT ONLY, BUS INTERFACE, FULL MAIL, I/O SCAN, and REDUCED MAIL. However, CPU Release 6.02 only supports NONE, BUS INTERFACE, FULL MAIL, and I/O SCAN modes. *The other modes should not be configured.*

Maximum PLC Sweep

In systems configured for IC66* Bus Redundancy a complete PLC sweep must be executed every 500 milliseconds or less, even though it is possible to configure the watchdog timer to higher limits. This also means that resetting of the watchdog timer with Service Request #8 cannot be done indefinitely.

Serial Communications

The following operating restrictions exist for the Serial Communications feature:

1. Serial communications can add up to 5 milliseconds of time to any given sweep. This should be taken into account when setting the watchdog timer.
2. The following procedure is recommended when changing baud rates in the PLC and the WSI board. First enter the configuration package and change the baud rate on the PLC, then store the new configuration. Now power off the PLC and then go to the WSI setup screen and change the WSI baud rate. Finally, power the PLC back on.
3. The link idle time setting in IC641 programming software *Config for Serial Communications* should be set to 10 seconds or greater. Otherwise a communications failure will occur when storing the config to the PLC.

There is a serial port configuration parameter under software configuration for the PLC called MODE. This configuration parameter can be one of two values: **SNP** to indicate that the serial port will be used for SNP communications, or **MSG** to indicate that the serial port will be used to send printf commands from a C program block to the connected device. If you have configured MODE to be **MSG** and are also using serial IC641 programming software as a means of communicating with the PLC, communications with IC641 programming software is lost when going to the RUN mode, since the serial port is currently configured for printf commands from C program blocks (or Standalone C programs).

IC641/WSI Attach

Do not connect or disconnect the WSI/BTM cable while the programmer host is powered-on. This action may cause a running PLC to Stop.

Expansion Rack ID

The expansion racks for the IC697 PLC are shipped with the rack ID strapped for rack 0 (the main rack). If the rack jumper is not changed the PLC will not recognize the rack at all and may not properly identify the error.

Expansion Rack Cable

Do not connect or disconnect the expansion rack cable while the CPU is running. This will cause the PLC to go to the STOP/HALT mode.

Expansion Rack Power

Expansion racks should be powered up at the same time that the main rack is powered up, or they should be powered up after the main rack has completed its power-up initialization. *Do not power-up an expansion rack while the CPU is running power-up diagnostics.*

Memory Usage

A general rule-of-thumb for memory usage is 48 bytes per I/O point plus register memory in bytes.

Timer Operation

Care should be taken when timers (ONDTR, TMR, and OFDTR) are used in program blocks that are NOT called every sweep. The timers accumulate time across calls to the sub-block unless they are reset. This means that they function like timers operating in a program with a much slower sweep than the timers in the main program block. For program blocks that are inactive for large periods of time, the timers should be programmed in such a manner as to account for this catch up feature.

Similar to this are timers that are skipped because of the use of the JUMP instruction. Timers that are skipped will NOT catch up and will therefore not accumulate time in the same manner as if they were executed every sweep..

I/O Link Interface

When powering up the PLC CPU without a battery, and I/O Link Interface boards are present, an incorrect *Loss of Module* fault will be logged for each I/O Link Interface board; but the PLC CPU will not consider these boards as lost, and the boards will continue to operate properly.

CommReqs with Retentive Memory

When powering up the PLC CPU with a program being retrieved from Retentive Memory and proceeding to RUN mode, any CommReqs to a PCM should be delayed for 5 seconds.

Constant Sweep

Constant Sweep time, when used, should be set to about 10 milliseconds greater than the normal sweep time to avoid any oversweep conditions when monitoring or performing on-line changes with the programmer. The smallest valid constant sweep time setting is 10 milliseconds for the Model 781, 782, 914, 915, 924, and 925 PLCs. Window completion faults will occur if the constant sweep setting is not high enough.

Interaction of IC641 Programming Software with Closed Programming Window

The IC641 programming software Sweep Control and Monitor screen cannot be used to change the PLC Sweep Modes or timers (Constant Sweep Time, Program Window Times, and others) while the program window is closed. Use Service Requests #1 through #4 to perform these functions.

SFC RESET Function

The SFC RESET function block only executes when used in the MAIN Ladder Diagram block. Attempting to execute an SFC RESET function block from a Ladder Diagram sub-block will not reset the SFC network and (as of version 6.02) will not pass power flow to any logic right of the SFC RESET.

Problems Resolved by This Upgrade

Lights out with No Faults or PLC CPU Hardware Fault with Programmer Access

Due to component timing tolerances and large ladder programs with certain sequences, SNP programmer port activity could have caused the CPU to suspend execution until a hardware watchdog timeout reset the board or a PLC CPU Hardware Fault occurred. Changes in the hardware were made to avoid the race condition that allowed the fault to occur.

New features and Functionality

There are no new features or functionality available from Release 6.00 to Release 6.01 and Release 6.02. The New Features and Functionality listed below are those that first appeared in Release 6.00 and are also provided in Release 6.02.

Standalone C Program

IC697 CPU Release 6.00 provides the ability to have PLC CPU application written exclusively in the C language. A standalone C program is called from the operating system directly – no Ladder Logic is required. Each standalone C program (code and data) can be a maximum of 512 Kbytes, providing there is sufficient RAM available on the PLC CPU.

A standalone C program can have up to eight input specifications and up to eight output specifications. Each input or output specification is defined as a start PLC memory reference and a data length. The input specifications are copied into the standalone C program when the standalone is scheduled for execution by the operating system. Output specifications are copied back to the specified PLC global memory upon completion of the standalone C program's execution. Each of the input / output specifications are defined by the user through IC641 programming software Release 6.00.

Standalone C programs are created using the C Programmer's Toolkit for IC697 PLCs (v3.00). For more information on Standalone C programs, please consult the *Programmable Controller Reference Manual* or *C Programmer's Toolkit for PLCs User's Manual.*

Multiple Programs

Release 6.00 of the IC697 PLC CPU now supports the storing of multiple programs to a single PLC. A maximum of 16 programs can be store to the Release 6.00 IC697 CPU. Of the 16, only one can be a Ladder Logic / SFC program. Therefore a Release 6.00 PLC CPU can take a maximum of one LD / SFC program and 15 Standalone C programs *OR* 16 Standalone C programs. The PLC CPU must still contain sufficient available User RAM to store all programs.

Embedded Debugger for C Applications

The IC697 CPU, beginning with Release 6.00, now includes a C debugger embedded in the CPU firmware. The embedded debugger is for use in debugging C applications running in the IC697 PLC CPU. Some of the capabilities provided by

the embedded debugger include the setting of hardware and / or software breakpoints, establishing watch variables, display / edit C application data, single step execution of the C application, and step-over / step-intoexecution control. The embedded debugger may be used to debug C (EXE) blocks and Standalone C programs in the Release 6.00 IC697 PLC CPU. Only one debug session is permitted at any time. When debugging a C application, start / stop control of the program is controlled through the embedded debugger, however, the IC697 PLC continues to execute its sweep – executing any other program in the CPU, scanning I / O, communicating with IC641 programming software (if connected), and communicating with any option modules (if present). A new C Toolkit, the PLC C Toolkit Professional (IC641SWP719A), is required to use the embedded debugger. The new C Toolkit provides the User Interface program for controlling the embedded debugger and the required communications drivers. Communications between the User Interface and the IC697 CPU is via SNP on the CPU's built-in serial port. (Note: Debugger communications drivers and User Interface program are DOS–based applications)

FIP I/O

The Release 6.00 IC697 CPU now supports FIP I / O (a new type of I / O network) and the FIP Bus Controller (FBC). For more information on FIP I / O and the FIP Bus Controller please refer to the *FIP Bus Controller User's Manual*.

Microcycle Sweep Mode

Microcycle is a new Sweep Mode of the Release 6.00 IC697 PLC CPU. In microcycle mode, each sweep begins at an absolute time relative to the STOP-to-RUN transition time. Programs are configured by the user to run at whole number intervals of the base cycle time. In microcycle mode the overall sweep is much like that of Constant Sweep, however, program execution can be *time sliced* over several sweeps. Higher priority (must run often) programs are given smaller intervals of the base cycle time, whereas lower priority (run less often) programs are given larger intervals. The interval defines how often the program will be scheduled for execution (e.g., an interval of 1 indicates that this program must execute every sweep. An interval of 3 indicates that the program should be scheduled for execution every third sweep.) Programs with interval 1 must be scheduled and complete execution every sweep. Programs with intervals greater than 1 are scheduled based on their interval, but execution of any given program need only complete prior to its next interval time to be scheduled. A program with interval 2 does not necessarily run 1 / 2 the program in one sweep and 1 / 2 in the next, and a program with interval 3 does not necessarily run 1 / 3 of its execution across 3 sweeps.

Note

The prior execution of a given program must complete before that same program can be scheduled for its next execution. If the program did not complete its prior execution, then at the time is to be scheduled, a fault will be logged and the program will not be scheduled on this interval.

Multiple SNP Sessions

The Release 6.00 IC697 PLC CPU now supports multiple logical connections through the CPU's built-in serial port. This functionality is provided in conjunction with the

Host Communications Toolkits to permit multiple user applications running in the same host computer to communicate serially (SNP) with the IC697 CPU via the Host Communications Toolkits and an SNP driver.

One Megabyte User Logic Memory

Beginning with IC697 PLC CPU Release 6.00, two new CPU models will be available: CPM915 and CPM925. Both of these models provide 1 Megabyte (1024 kilobytes) of User Logic memory. These CPUs support multiple programs with the restrictions that no single program can be larger than 512 Kbytes and only one LD / SFC program is permitted. IC641 programming software Release 6.00 is required to configure these new CPU models.

CPM915 and CPM925

These are two new IC697 PLC CPU models with each providing 1 megabyte of user logic memory. (Please refer to above discussion of new 1 Megabyte User Logic Memory option for details.)

FIP Device Status References (F_rsnnn)

With the addition of FIP I / O to the Release 6.00 IC697 CPU, we have included FIP device status references. These FIP device status references are analogous to the Module status references provided for use with GENIUS bus based devices (M_rsbmm). FIP device status references take the form:

F_rsnnn

where: **F** indicates this is a FIP device status reference
r indicates the VME rack number of the FIP Bus Controller
s indicates the VME slot number of the FIP Bus Controller
nnn indicates the node id of the FIP I / O nest

The FIP device status references are to be used with the FAULT and NOFLT contacts to determine if an I / O nest on the FIP I / O network has a fault condition.

Interrupt Blocks Calling Other Blocks

Previous releases of the IC697 PLC CPU have not permitted calls to other blocks from within an LD block configured as an I / O or Timed Interrupt Block. This restriction has been removed with Release 6.00.

14-Point Interrupt Module

Support for the IC697 14-point Interrupt Module has been incorporated into the Release 6.00 IC697 PLC CPU. Use of the 14-point Interrupt Module with prior versions of the IC697 PLC CPU required application support from within the user's logic program to interface with and control the 14-point Interrupt module. This support is now in the CPU firmware.

Note

When upgrading to IC697 CPU Release 6.00, the PLC logic associated with supporting the 14-point Interrupt Module ***MUST*** be removed from the application program prior to placing the Release 6.00 CPU into RUN mode. If this support logic is not removed, incorrect operation of the 14-point Interrupt Module, the application program, and the IC697 PLC CPU firmware will result.

Boot Loader Enhancements (CPM915 and CPM925)

Included as part of the Release 6.00 upgrade is an enhancement to the Boot Loader functionality of the CPM915 and CPM925. The Boot Loader is contained in a separate EPROM on the CPM915 and CPM925 motherboard. The Boot Loader is used in conjunction with the PC Loader (DOS based utility program) to perform updates to firmware that is in FLASH memory. This Boot Loader enhancement prevents the downloading of incorrect firmware FLASH programs to the target CPU board. Previously it was possible to download an incorrect FLASH program to a CPM914 or CPM924 CPU and the incorrect program was not detected until the very end of the download. The resulting update would cause the CPU to remain in Boot Mode until a valid update was performed.

The new Boot Loader on all CPM915 and CPM925 modules (when used with PC Loader version 3.10) will verify that the firmware update to be downloaded is appropriate for the target CPU ***prior*** to initiating the download.

PID Function Block

V6.02 firmware now provides support (based upon the PID function block configuration word) for anti-reset windup action. The PID configuration word allows you to select whether PID should back calculate the result (DEFAULT action) or pre-clamp reset hold. Please refer to *Additions to the Reference Manual* for a detailed description of the updated PID function block configuration word.

Note

The described changes in the PID config word were actually provided, but not documented, in version 6.01 CPU firmware. If you currently have version 6.01 firmware, the described anti-reset windup action of the PID function block is available.

Restrictions and Open Problems

1. If an expansion rack powers up while the CPU in the main rack is in the RUN mode, the slot fault contacts will prematurely indicate that the modules in the expansion rack are not faulted *before* they complete their power up.

2. In a multi-rack system, false LOSS OF RACK faults may occur when the system loses power. If this fault is configured to be fatal, the system will power-up in STOP mode.

3. When there is no logic stored in a CPU module the %Q and %M tables will be cleared when the CPU is placed in RUN mode. In this context *no logic stored* means that no program had ever been stored or that the clear function on the IC641 programming software had been used to clear logic and configuration.

4. When the Bit Sequencer sequences from one step to another, the negative transitional contact that corresponds to the original step is not set. The transition contact for the new step is set and remains set until the sequencer sequences to the next step. This operation is identical to the operation of the previous versions of the CPU firmware.

5. If multiple faults exist in an IC697 PLC remote drop and one of them is corrected, a FAULT contact that uses the remote drop's module reference will incorrectly indicate that no faults exist at the remote drop.

6. An Analog Input Base module and its expander modules may not come online if they are configured in an expansion rack that is missing when the main rack powers up. Power-up the expansion rack first, then power-up the main rack.

7. If the main rack loses power during PLC configuration, analog input base boards (IC697ALG230) in expansion racks that do not lose power may fail. The failure would occur on the subsequent configuration. PLC configuration occurs during power up, store of configuration, and reads from Retentive (Flash) Memory. To prevent the failure, tie all racks to a common power source. To correct the failure, power-cycle the expansion racks.

8. If the CPU is to power-up into RUN mode the full power-up diagnostic tests are supposed to be skipped. If *only* an I/O configuration (no program) is stored to the PLC and the PLC is placed in RUN mode, then a power-cycle of the PLC will result in the CPU performing its full power-up diagnostic tests.

9. Care must be taken when using continuation coils/contacts in the main LD program execution and also in interrupt block execution. There is only one location in Bit Cache memory for storing the continuation coil. Because of this do not use continuation coils/contacts in both main LD program and in interrupt blocks.

10. An incorrectly formatted COMMREQ (for example, incorrect task id field) directed to a PCM or CMM module does not result in an error being logged in the PLC fault table. Correctly formatted COMMREQs operate normally.

Additions to the PLC Reference Manual

IC697 Instruction Set: SVCREQ #15

Page 4-214 of the G version of the *Programmable Logic Controller Reference Manual* provides a description of the returned data when a SVCREQ #15 is executed (read last fault). The number of bytes of meaningful fault specific data varies depending on whether the logged fault is long or short and also whether it is an I/O fault or a PLC fault.

Referring to the fault table descriptions on page 4-213 and 4-214, the Long/Short indicator (in the least significant byte of word address + 1) defines the number of bytes of meaningful fault specific data present in the fault memory. Defined values are:

Fault Table Type	Long/Short Value
PLC Fault Table	00 = 8 bytes (short)
	01 = 24 bytes (long)
I/O Fault Table	02 = 5 bytes (short)
	03 = 21 bytes (long)

IC697 Instruction Set: PID

The PID function block has been enhanced in version 6.02 to make the anti-reset windup mechanism configurable. Prior to this release, the IC697 CPU would back calculate the reset term whenever the output is clamped. In version 6.02 this is now the DEFAULT mechanism. Alternatively, you can now choose to simply hold the reset term at its pre-clamp value. The advantage of the new mechanism is to reduce overshoot caused by the reset term as a result of a step change to the SP.

Note

The described changes in the PID config word were actually provided, but not documented, in version 6.01 IC697 CPU firmware. If you currently have version 6.01 firmware, the described anti-reset windup action of the PID function block is available.

Example: A process is in steady state with PV=58 degrees. A batch is turned on and SP is jumped to 200 degrees. The output clamps high and, with the default anti-reset back calculation, the reset term is driven low to prevent the output from exceeding the clamp. When the PV comes up near the SP, the reset term is large and negative because of the back-calculation. This term must be integrated out, which takes times, so the process overshoots. The new method, if configured, would simply hold the original pre-clamp reset term, presumably small, so it does not take any time to integrate out, thereby reducing overshoot.

Page 4-241 of the *Programmable Logic Controller Reference Manual* provides a description of the defined bits in the PID configuration word. This bit definition is contained in Table 4-4 PID Function Block Data. The configuration word has been enhanced in version 6.02 firmware to include support for an anti-reset windup action (as described above) and Table 4-4 (below) shows the version 6.02 firmware definitions for the PID function Block configuration word.

Table 4-4. PID Function Block Data

Data Item	Description
Config Word	A word value with the following format: bit 0 = Error Term. When this bit is set to zero, the error term is SP-PV. When this bit is set to 1, the error term is PV-SP. bit 1 = Output Polarity. When this bit is set to zero, the CV output represents the output of the PID calculation. When it is set to 1, the CV output represents the negative of the output of the PID calculation bit 2 = Derivative action on PV. When this bit is set to zero, the derivative action is applied to the error term. When it is set to 1, the derivative action is applied to PV. All remaining bits should be zero. bit 3 = Deadband action. When the Deadband action bit is set to zero, then no deadband action is chosen. If the error is within the deadband limits, then the error is forced to zero. Otherwise the error is not affected by the deadband limits. If the Deadband action bit is set to 1, then deadband action is chosen. If the error is within the deadband limits, then the error is forced to be zero. If, however, the error is out side the deadband limits, then the error is reduced by the deadband limit (error = error - deadband limit). bit 4 = Anti-reset windup action. When this bit is set to zero, the anti-reset windup action uses a reset back calculation. When the output is clamped, this replaces the accumulated Y term with whatever value is necessary to produce the clamped output exactly. When the bit is set to one, this re places the accumulated Y term with the value of the Y term at the start of the calculation. In this way, the pre-clamp Y value is held as long as the output is clamped. NOTE: The anti-reset windup action bit is only available on release 6.01 or later CPUs.

Instruction Timing

Table A-1 below contains updated information for several of the IC697 CPU instruction timings. These updates apply to those numbers given in the *Programmable Controller Reference Manual*, in appendix A.

Table A-1. Instruction Timing

Function Group	Function	Enabled				Disabled				Increment				Size
		924/925	914/915	781/782	731/732 771/772	924/925	914/915	781/782	731/732 771/772	924/925	914/915	781/782	731/732 771/772	
Relational	RANGE(INT)	9	11	33	–	3	4	12	–	–	–	–	–	18
	RANGE(DINT)	10	13	38	–	3	5	12	–	–	–	–	–	18
Bit Operation	AND (WORD)	16	19	61	116	5	7	26	35	0.5	0.5	8.0	18.0	18
	OR (WORD)	15	19	62	118	6	7	26	35	0.5	0.5	9.0	19.0	18
	XOR (WORD)	7	19	58	118	5	7	23	35	0.5	0.5	9.0	19.0	18
	NOT (WORD)	10	13	40	76	5	6	23	32	0.4	0.5	3.0	8.0	15
	NOT (DWORD)	8	12	40	79	6	7	22	31	0.1	0.5	3.0	10.0	15
	MCMP (WORD)	19	23	98	212	7	11	36	58	0.6	1.0	3.0	8.0	30
	SHL (WORD)	11	17	63	137	5	8	30	41	0.6	1.0	4.0	10.0	24
	SHR (WORD)	12	19	64	138	5	9	27	42	0.5	1.0	4.0	10.0	24
	ROL (WORD)	12	16	57	119	5	6	24	53	0.5	1.0	4.0	9.0	18
	ROR (WORD)	9	15	53	113	5	6	23	34	0.6	1.0	4.0	9.0	18
	MOVE (BIT)	13	19	58	119	5	7	20	32	0.8	1.0	3.0	6.0	15
	BPOS (WORD)	9	15	55	107	5	7	25	35	0.2	0.5	1.0	4.0	18
	BPOS (DWORD)	13	20	81	158	5	8	23	36	0.2	0.5	3.0	6.0	18
Array	ARRAY_RANGE (WORD)	13	17	53	–	4	5	14	–	0.9	1.0	1.4	–	21
	ARRAY_RANGE (DWORD)	13	18	53	–	4	5	14	–	0.9	1.0	3.9	–	21
Control	SVCREQ:									–	–	–	–	12
	#23	74	98	302	–	2	3	10	–	–	–	–	–	12
	#25	19	26	79	–	2	4	10	–	–	–	–	–	12
	#32	42	52	148	–	3	4	10	–	–	–	–	–	12

1. Time (in microseconds) is based on Release 6.0 of IC641 programming software software ("–" indicates value not available, not applicable, or not supported with Release 6.0)
2. For table functions, increment is in units of length specified. For bit operation functions, microseconds / bit. For data move functions, microseconds / the number of bits or words.
3. Enabled time is for single length units of type %R.

I/O Interrupt Rate Limits

Table A-13 and A-14 (below) contain updated information for the IC697 CPU interrupt rate limits. These updates apply to those numbers given in the IC697 *Programmable Controller Reference Manual* in Appendix A.

Table A-13. I/O Interrupt Performance

	CPU Model			
	771/772[1]	781/782	914/915	924/925
Maximum Interrupt Rate with IOMs	450 interrupts per second	900 interrupts per second	2250 interrupts per second	2250 interrupts per second
Maximum Interrupt Rate without IOMs	750 interrupts per second	1600 interrupts per second	3750 interrupts per second	3750 interrupts per second

Table A-14. Event-Triggered Interrupt Program Performance

	CPU Model			
	771/772[1]	781/782	914/915	924/925
Maximum Interrupt Rate with IOMs	n/a	750 interrupts per second	2150 interrupts per second	2250 interrupts per second
Maximum Interrupt Rate without IOMs	n/a	1300 interrupts per second	3600 interrupts per second	3750 interrupts per second

[1] Values are based upon release 5.00 PLC CPU firmware.

Sweep Impact Timing Test Results

	CPU781/782		CPM914/915		CPM924/925	
	With Point Faults Disabled (ms)	With Point Faults Enabled (ms)	With Point Faults Disabled (ms)	With Point Faults Enabled (ms)	With Point Faults Disabled (ms)	With Point Faults Enabled (ms)
Base Sweep Time	702.5	702.5	207.4	207.4	152.5	152.5
Rack Setup per expansion Rack	1.0		0.5		0.5	
I/O Scan Overhead	175.6	196.9	138.2	148.0	134.8	141.2
Per Discrete I/O module in main rack	20.9	28.3	10.5	15.6	9.0	13.6
Per Discrete I/O module in expansion rack	22.6	39.8	11.0	18.3	10.2	14.9
Per Discrete Fault		425.6		157.0		118.9
Per Analog I/O module in main rack	27.9	30.8	16.0	22.3	14.9	20.7
Per Analog I/O module in expansion rack	48.0	76.1	31.8	52.3	32.1	46.4
Per Analog Input Expander in main rack in same segment	18.8	27.5	16.9	25.9	15.2	24.2
Per Analog Input Expander in same segment in expansion rack	57.0	85.6	56.7	83.6	55.8	82.4
Per Analog Input Expander in new segment in main rack	36.6	51.4	22.7	32.4	20.3	27.9
Per Analog Input Expander in new segment in expansion rack	70.5	104.7	65.3	93.4	59.8	88.3
Per Analog Fault	936.2		329.6		259.7	

	CPU781/782		CPM914/915		CPM924/925	
	With Point Faults Disabled (mꝛ)	**With Point Faults Enabled (mꝛ)**	**With Point Faults Disabled (mꝛ)**	**With Point Faults Enabled (mꝛ)**	**With Point Faults Disabled (mꝛ)**	**With Point Faults Enabled (mꝛ)**
GBC Open System Comm. Window	189.0		61.6		43.2	
per GBC polling for Background Messages	20.0		8.6		8.1	
per GBC I/O Scan	811.0		647.6		423.7	
Genius I/O Block per I/O block scan segment	44.4	72.5	30.0	60	27.0	54.0
Genius I/O Block per byte discrete I/O data main rack	3.1	4.3	1.7	3.4	1.5	3.0
Genius I/O Block per byte discrete I/O data exp. rack	4.5	15.3	2.5	4.0	2.0	4.2
Genius I/O Block per word analog I/O data main rack	4.2	9.1	1.1	1.6	1.1	1.6
Genius I/O Block per word analog I/O data exp. rack	13.1	16.0	5.7	9.33	4.0	6.0
FIP I/O Block per I/O block scan segment	29.0	67.0	11.6	15.3	11.4	11.9
FIP I/O Block per byte discrete I/O data main rack	2.5	4.8	2.4	2.9	1.9	2.9
FIP I/O Block per byte discrete I/O data exp. rack	4.4	6.4	2.6	3.3	2.4	2.8
FIP I/O Block per word analog I/O data main rack	7.1	8.8	1.1	1.9	0.8	1.8
FIP I/O Block per word analog I/O data exp. rack	9.8	13.1	3.2	5.8	4.3	4.9
PLC Memory Access from IOMs – Read/Write 1 to 3 words	1206		445		399	
PLC Memory Access from IOMs – Read/Write 4 to 128 words	1393		579		483	
PLC Memory Access from IOMs – Read/Write each additional 128 words	1835		803		653	
Clock Refresh Rate	324.8		145.5		138.6	
LAN module I/O Scan Time	66.5		58.6		47.1	
I/O Interrupt Minimum Response Time	675	778	359	370	313	326
I/O Interrupt Typical Response Time	679	797	363	386	316	331
I/O Interrupt Maximum Response Time	1633	1734	772	783	627	640
Timed Interrupt Minimum Response Time	227	318	147	151	108	113
Timed Interrupt Typical Response Time	346	403	185	195	143	150
Timed Interrupt Maximum Response Time	464	507	219	229	163	166